PROJECT RESULT

Technology platform for next-generation core CMOS process

MEDEA+

2T101: Strained silicon on insulator substrates for high performance ICs (SilOnIS)

Advanced substrate engineering drives future device performance

Silicon-on-insulator (SOI) architectures offer semiconductor manufacturers higher speeds and lower consumption than bulk silicon, while strained silicon improves performance further. The SilOnIS project built on the strengths of the main European players in substrates, chipmaking and metrology to combine high mobility wafer-level strained silicon and SOI architectures in a single technology platform for high performance chips. The project set out to develop large diameter strained SOI substrates, suitable for 45 nm and below technology fabrication, as a first step in engineering advanced substrates.

Improving charge carrier mobility – as a simple image the rapidity at which particles carrying the electrical flow in an electronic device can react to an electrical field – is a top technical priority for the CMOS community in both high performance and low power applications. This requires innovative solutions to meet mandatory future needs where traditional solutions appear to be limited. The International Technology Roadmap for Semiconductors (ITRS) clearly reflects the universality and importance of this topic.

A family of solutions is already known, based on the application of a strain field – tensile or compressive – to the semiconductor active layer of the transistor, resulting in an increase of charge-carrier mobility. While such solutions have been implemented in production lines for current technology nodes, they cannot easily follow future requirements established by the ITRS.

However, another technological breakthrough – silicon on insulator (SOI) – has emerged over the past decade related to the use of very thin films of semiconductor layers, which can increase the rapidity of devices or lower their power consumption.

Single platform

The MEDEA+ 2T101 SilOnIS project set out to develop an alternative solution by providing an industrial source of large diameter substrates combining high mobility 'strained' silicon (Si) and SOI technologies in one single technology platform in the form of strained SOI (sSOI) substrates. The project bought together the main European actors in the fields of substrate materials, metrology and chipmaking and covered both materials development and early validation in devices.

SilOnIS called for many elementary technical leading-edge developments such as: epitaxy of strained Si and silicon-germanium (SiGe); dislocation engineering for strain relaxation; 'Smart Cut™' layer transfer technology applied to SiGe/strained Si; strain engineering at substrate level; combination of uniaxial and biaxial strain fields in the channel; and transistor fabrication adapted to ultra-thin and strained films.

Main results included:

- Demonstration of sSOI substrates in 200 and 300 mm diameter wafers;
- Dislocation density improvements over several orders of magnitude;
- Substrate quality improvements in line with the target, with some parameters already reaching standard SOI quality or even better;
- Demonstration of specific sSOI types addressing different transistor architectures and nodes;
- Demonstration of scalability at substrate level with a second generation in terms of strain value;

- Preliminary second generation sSOI already at similar defectivity level to first generation;
- Transistor demonstration both on partially depleted SOI for high performance and fully depleted SOI for low power applications;
- Demonstration of +35% Ion for FD SOI in NMOS; and
- Demonstration of NMOS and PMOS gain for both first- and second-generation sSOI substrates.

Broad impact

The impact of SilOnIS has been broad considering the different segments of the microelectronic food chain it covers:

1. Substrates and materials actors – the expected impact is clear on the substrate suppliers involved, reinforcing their leading position in this new high added value segment of engineered substrates. It has provided the European suppliers with an excellent opportunity to counterbalance Japanese companies' lead in the bulk silicon market. But it also concerns European equipment suppliers, especially in the field of advanced epitaxy, since SiGe and strained Si epitaxy are at the centre of such a technology, with some specifics when applied to sSOI substrates.
2. Semiconductor manufacturers – the objective was to improve charge carrier mobilities for future technological nodes. Being involved early in innovative solutions such as those proposed by SilOnIS is of prime importance, and the success of this project will strengthen the position of European semiconductor companies. Being related to low power and high performance applications, the expected impact of this project will concern several major players.
3. Specific metrology – both for substrates and for devices, the new sSOI structure calls for specific metrology or specific ways of using standard metrology. Several complementary metrology and characterisation equipment suppliers have been associated with this project, enabling each of them to be involved in these leading edge evolutions and ultimately enrich their equipment portfolio.

Multiple reuse

SilOnIS involved innovation at both material and substrate levels but was device driven from the start. A particular advantage is that the MEDEA+ project addressed more than one ITRS node as multiple reuse of results is possible as dimensions continue to reduce.

As a result of the project, industry-standard 300 mm diameter wafers of thin and thick strained SOI prototype substrates were delivered to the chipmaking partners for device development. These wafers could be used in existing processing equipment. And suitable wafers have been demonstrated targeting device fabrication at the 45 nm half-pitch node and below, in line with global industry needs.

This MEDEA+ project marks a first step in the engineering of advanced substrates for integrated circuit production. Europe has a strong position in this field and, by supporting work in this area, SilOnIS has participated in the recognition of a field of activity that can become another future European strength. The results will not only boost the companies involved directly but also the ecosystems with which they are involved, benefiting employment and spreading knowhow in this important emerging field.

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PARTNERS:

Aixtron
AMD Saxony
ASM
CEA – LETI
Freescale (formerly MOTOROLA)
Infineon (in 2005)
JOBIN YVON
NANOMETRICS
NXP
OMI
Siltronic
SOITEC
SOPRA
STMicroelectronics

PROJECT LEADER:

Bruno Ghyselen
SOITEC

KEY PROJECT DATES:

Start: January 2005
End: December 2007

COUNTRIES INVOLVED:

France
Germany
Ireland
The Netherlands
UK

MEDEA+ Office
140bis, Rue de Rennes
F-75006 Paris
France
Tel.: +33 1 40 64 45 60
Fax: +33 1 40 64 45 89
Email: medeaplus@medeaplus.org
http://www.medeaplus.org

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MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon.